AlN COATED HETEROJUNCTION FIELD EFFECT TRANSISTOR AND METHOD OF FORMING AN AlN COATING

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Cross-Reference to Related Applications

This application claims priority to U.S. Provisional Application Serial No. 60/278,566, filed March 23, 2001, the specification of which is hereby incorporated by reference.

Field of the Invention

The present invention relates to heterojunction field transistors, and in particular to the use of AlN to coat such transistors for improved performance and to a method of forming an AlN coating.

Background of the Invention

Many electronic devices utilize field effect transistors for amplifiers. heterojunction field effect transistors (HFETs) have been used for high frequency amplifiers, such as for microwave transmissions. As wider bandwidth signals of greater complexity are transmitted, larger bandwidth of greater complexity are transmitted, larger bandwidth amplifiers are required to transmit them. The most common approach to broad bandwidth is to take a high power narrow band amplifier design and make it broadband by sacrificing power for bandwidth. The only way to boost the broadband power back to narrowband levels is to use a higher power amplifier transistor. GaN is a desired choice for higher microwave power transistors. GaAs transistors have also been used to less extent. GaN is a fundamentally higher power choice because it is larger bandgap which

permits higher voltage operation, and higher temperature operation than GaAs. It is also more chemically stable than GaAs which gives it advantages in reliability.

Beyond high power amplifiers, there is a need for GaN receiver transistors because they can survive unintentional exposure to high voltages. For example, if something passes directly in front of a transmitting radar, the reflected beam back to the radar receiver can burn out the receiver front-end transistor.

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There is a need for increasing the power output of HFETs. Prior attempts include using a layer of Si3N4 over the surface of an already formed HFET. While this improved the power output of the HFET, it required different equipment than was used to form the HFET. Further, controlling the ratios of the deposition required careful calibration and it was difficult to obtain consistent results.

Summary of the Invention

An AlN passivation layer is applied to the surface of heterojunction field effect transistors (HFET)s. The deposition follows all other transistor processing steps in one embodiment.

In one embodiment, the passivation layer of AlN is deposited on a GaN channel HFET using molecular beam epitaxy (MBE). Using MBE, many other surfaces may also be coated with AlN, including silicon devices, nitride devices, GaN based LEDs and lasers as well as other semiconductor systems.

The deposition is performed at approximately 150°C and uses alternating beams of aluminum and remote plasma RF nitrogen to produce an approximately 500Å thick AlN layer. The temperature and thickness may be varied as desired. At temperatures about or higher than 300°C, melting may occur, damaging the integrity of the HFET. Lower temperatures may also be used, and in fact may provide desired poly-crystalline characteristics.

Other methods of applying the passivation layer may also be utilized, including sputtering. In one embodiment, alternating periods of deposition of Al and N are approximately two seconds in length, with two second intervals between the depositions. The times may be varied significantly, but approximate migration enhanced epitaxy,

which may also be used. Such deposition provides highly conformal coverage of the passivation layer on the gate.

HFETs with AlN passivation layers are useful in a wide range of products, including microwave generated plasma lights, microwave transmitters, receivers, cellular base stations, microwave ovens, home to satellite transceivers, and collision avoidance radar for automobiles to name a few.

Brief Description of the Drawings

Figures 1, 2, 3, 4, 5, 6, 7 and 8 are block cross sections of a number of fabrication steps that are employed to fabricate a GaN based FET having an AlN passivation layer formed in accordance with the present invention.

Figure 9 is a block cross section of a complete FET having the AlN passivation layer formed thereon.

Detailed Description of the Invention

In the following description, reference is made to the accompanying drawings that form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that structural, logical and electrical changes may be made without departing from the scope of the present invention. The following description is, therefore, not to be taken in a limited sense, and the scope of the present invention is defined by the appended claims.

A passivation layer of AlN is applied to the surface of GaN channel heterojunction field effect transistors (HFET)s or other semiconductor devices or optoelectronic devices as an optical coating by molecular beam epitaxy in one embodiment. The deposition follows all other transistor processing steps. In one embodiment, the deposition is performed at 150°C using alternating beams of Al and remote plasma RF nitrogen to produce an approximately 500Å thick AlN layer. Less thick layers may be used, and a thickness of approximately 2000Å may also be used,

especially for integrated capacitors. It should also be noted that other types of transistors, such as metal semiconductor field effect transistors (MESFETs) and high electron mobility transistors (HEMTs) also benefit from the passivation layer.

In one example, addition of the AlN passivation or surface layer approximately doubled the output power of HFETs in the 8 GHz range. RF output current increased from 400mA/mm to 800mA/mm. Vds breakdown Results may vary, and the above example is not a guarantee of performance. AlN can be deposited with great accuracy in Al to N ratio (1:1) with ease, resulting in increased yield over the use of prior passivation layers. It may also be applied using the same equipment used to fabricate the HFET. This enables the passivation layer to be applied without moving wafers to different machines. AlGaN transistors, silicon devices, nitride devices, GaN based LEDs and lasers as well as other semiconductor systems. may also be passivated in the same manner.

Heterojunction Field Effect Transistors (HFET)s made from GaN are useful for application to high power microwave amplifiers. While large channel currents and high breakdown voltages are seen for 2 dimensional electron gas (2DEG) HFETs compared to transistors made from GaAs and other related materials, these large DC channel currents are usually not obtained as peak channel currents under RF modulation. This characteristic is common for GaN HFETs which utilize 2DEGs that result from spontaneous polarization and piezoelectric induced electrons.

Further uses include broadband RF amplifiers for microwave transmissions. As wider bandwidth signals of greater complexity are transmitted, larger bandwidth amplifiers are required to transmit them. The most common approach to broad bandwidth is to take a high power narrow band amplifier design and make it broadband by sacrificing power for bandwidth. The only way to boost the broadband power back to narrowband levels is to use a higher power amplifier transistor. GaN is a fundamentally higher power choice because it has a larger bandgap which permits high voltage operation, and high temperature operation. It is also chemically stable which gives it advantages in reliability.

Beyond high power amplifiers, there is a need for GaN receiver transistors because they can survive unintentional exposure to high voltages. For example, if something passes directly in front of a transmitting radar, the reflected beam back to the radar receiver can burn out the receiver front-end transistor.

Future uses include broadband phone/video/wireless in the commercial arena. These include terrestrial base stations and consumer satellite applications. Much higher bandwidth communications from home to satellite would become economical with GaN transistors.

Low cost high power microwave transistors may also enable new sources of lighting. A microwave generated plasma is a very efficient source of high intensity light with a superior color distribution - more like sunlight. Automobile headlights and medical uses such as operating room lighting would also benefit. Cheap high power transistors could even end up replacing the klystron tubes in consumer microwave ovens.

Low cost millimeter wave transistors that can survive wide temperatures of operation are also required for collision avoidance radar for cars. Automobile manufacturers are looking at GaN as a reliable material for this application.

Figures 1-9 are schematic illustrations of a number of fabrication steps that are employed to fabricate a GaN based FET in one embodiment, with Figure 9 showing a passivation layer of AlN formed thereon in accordance with one embodiment. The exact manner of formation of an FET may be done in many different ways, and is in no way intended to be limited by the embodiment described.

A FET 10 is formed on a substrate 12 in Figure 9. Numbers referring to the same features in different figures are consistent between the figures. Figure 9 shows the finished FET 10 with passivation layer, and it is first described, followed by a description of the intermediate steps illustrated by Figures 1-8. Substrate 12 can be any suitable material, such as sapphire, SiC, GaN, Si, etc. A buffer layer 14, formed from GaN in one embodiment, and a barrier layer 16, which is made of undoped AlGaN in the case of an HEMT, and doped GaN in the case of a MESFET, are formed on the substrate 12. Together, these form a mesa 18 that serves to isolate the FET from other FETs (not shown) on substrate 12.

A source ohmic contact 20 and a drain ohmic contact 22 are disposed on top of the barrier layer 16 for making electrical connections to a source 24 and a drain 25 respectively, that are formed in the barrier layer 16. A channel region 23 is thus formed between the source 24 and the drain 25 near the top surface of the buffer layer 14 adjacent the interface between the buffer layer 14 and the barrier layer 16, as is conventional. A gate 26 is also disposed on the barrier layer 16 between the source and the drain contacts 20 and 22. First and second metal interconnects 28 and 30, which are formed from gold in one embodiment are disposed on the source and drain contacts 20 and 22, respectively.

The AlN passivation layer 32 is disposed on top of the exposed surface of the barrier layer 16 between the source and drain contacts 20 and 22. A resist layer 34 and an airbridge metallization 36 comprised of a priming metal layer 38 and a plated gold layer 40 are optionally formed. The airbridge 36 provides a multi-level interconnect scheme as well as a top plate 42 to a metal-insulator-metal (MIM) capacitor 44, and a bottom plate 46.

To fabricate the FET 10, a buffer layer 14 and the barrier layer 16 are grown on the substrate 12 using an epitaxial growth process, such as organo-metallic vapor phase epitaxy, or molecular beam epitaxy (MBE). Next, as illustrated in Figure 1, the definition of the active msa 18 is performed using a first photo resist mask 50 and dry etching. Once the photo resist mask 50 has been patterned, the mesa 18 is etched using either reactive-ion etching (RIE), electron-cyclotron resonance etching (ECR), or wet chemical etching, to etch the AlGaN/GaN barrier layer 16 and all or part of the GaN buffer layer 14.

In Figure 2, the resist mask 50 used for etching the mesa 18 is removed and resist is applied and patterned to form a second resist mask 52 which defines a "lift-off" profile for definition of the ohmic contact metalization for the source and drain contacts 20 and 22. After resist patterning, a Ti/Al/Ti/Au metal stack multilayer 54 (shown as one layer) is deposited by evaporation or some other means. After evaporation, solvents are used to dissolve the resist beneath the ohmic contact metal stack and hence lift off the overlaying metal in all areas other than where the multilayer 54 is deposited on the barrier layer 16.

Following the removal of resist and excess metal, high temperature annealing (e.g., 800°C for 30 seconds) is used to diffuse the aluminum in the metal stack multilayer 54 into the AlGaN barrier layer 16 to form the ohmic source and drain contacts 20 and 22.

After the formation of ohmic contacts 20 and 22, another resist layer 56 is then deposited and patterned for formation of the gate 26 as shown in Figure 3. The resist layer 56 is exposed and developed using either optical or electron beam lithography. After the patterning of the gate 26 in the resist layer 56, a Ni/Au metal stack 58 is deposited to form a rectifying contact to the AlGaN barrier layer 16. Figure 3 shows a typical electron beam lithography process whereby the resist is exposed and developed to form the gate 26 in the shape of a "mushroom" whose large cross-sectional area minimizes the gate's electrical resistance. As in the case of the ohmic contact fabrication step, the excess metal is removed using the lift off technique as shown in Figure 4, thereby leaving the gate 26 exposed between the source and drain ohmic contacts 20 and 22.

Deposition of the conductors for circuit connections and capacitor electrodes takes place after gate metallization as shown in Figure 5. This step consists of patterning a photo resist layer 60, again using a lift off profile, depositing a metal layer 62, and then lifting off the excess metal using solvents. The deposited metal consists of a titanium adhesion layer and gold for low-resistance interconnects.

Following the deposition and patterning of the interconnect metal, the thin passivation layer of AlN is formed over the entire device wafer as shown in Figure 6 and discussed in more detail below. After forming the passivation layer 32, photoresist is deposited and patterned to form an etch mask 64 defining windows in the passivation layer for electrical connections as illustrated in Figure 7. Etching of AlN is performed by wet chemical etch, such as using KOH or HF. It may also be etched using a plasma etching process. The AlN can also be scratched through to the metal pads for testing.

Formation of the airbridges 36 shown in Figure 9 follows the deposition and patterning of the passivation layer 32. In Figure 8, this step consists of first, the deposition of the thin priming metal layer 38 on top of a layer of resist 66 patterned with holes where electrical contacts to the devices are made. After the deposition of the

priming metal layer 38, another level of resist is added to define the airbridges 36. Finally, the gold layer 40 is plated on top of the primer metal layer 8 to complete the airbridge spans 36 as shown in Figure 9.

AlN as a surface passivation layer for GaN HFETs increases the output power. Molecular beam epitaxy (MBE) is used in one embodiment to grow AlN at 150°C. The MBE technique is used in the migration enhanced epitaxy (MEE) mode in an attempt to provide the best possible sidewall coverage surrounding the gate.

In one embodiment, GaN HFET epitaxial layers are grown using MBE. The HFETs are fabricated with 0.3x100μm T-shaped gates. A wafer on which the HFETs are formed has a 300K Hall mobility of 1450 $cm^2/Vsec$ and electron sheet density of $1.1x10^{13}$ cm^{-2}. This embodiment is just one example, and should not serve to limit the invention, as the benefit of the passivation layer may be obtained over a wide variety of parameters.

In a further embodiment, AlN is deposited on HFET devices that are contained on 1.2x1.2cm processed wafer. The wafer is cleaned with solvents and receives a short dip in dilute HF to remove surface oxide. It still has a 1-micron thick tungsten coating on the back of the sapphire from the original MBE growth. The wafer is outgassed at 100°C for 1 hour in vacuum before transfer into the MBE growth chamber. The AlN growth rate is 800Å/hour. The RF plasma source is run at 350W, 0.7sccm N_2 flow and produces a background pressure of approximately $1.0x10^{-5}$T in a turbomolecular pumped Intevac® GEN II machine.

Growth takes place at a substrate temperature of 150°C as measured by a substrate heater thermocouple. Al and N are opened for alternating 2-second periods, with 2 seconds of growth interruption between each opening. This technique is an approximation of migration-enhanced epitaxy (MEE). The substrate temperature here is presumed to be too low for growing single crystal AlN. Single crystal AlN is avoided because of the possibility that it could cause the existing AlGaN barrier to become strained beyond critical thickness with the GaN HFET channel. This would remove the piezoelectric induced 2DEG, and form dislocations that could further harm the HFET

characteristics. In addition, a single crystal AlN layer could form an unwanted 2DEG at the surface of the HFET due to spontaneous polarization.

In further embodiments, poly-crystalline or amorphous forms are obtained. The structure of the crystals may be wurtzite or cubic.

MEE was chosen as an alternative to MBE for 2 reasons. First, MEE can be used to grow high quality materials, such as GaAs, at lower substrate temperatures than MBE because of enhanced surface migration of group III atoms in the absence of a group V flux. The low temperature requirement of the existing device structures makes MEE possibly more attractive. The second reason for choosing MEE is the possibility that better sidewall coverage, especially along the side of the gate, might be possible. Ga atoms preferentially migrate to the intersection between vertical features and the horizontal wafer surface.

One theory of the effect of surface nitrides deposited on HFETs is that the most important aspect of surface coverage is to better confine the electrical extension of the gate along the surface. For this reason, it is presumed that close contact, and lack of voids, along the side of the gate are important for effective surface modification.

In order to be a useful surface modification technique, AlN deposition should not cause significant degradation of other useful device properties.

Conclusion

An AlN passivation layer is applied to the surface of heterojunction field effect transistors (HFET)s. The deposition follows all other transistor processing steps in one embodiment. The deposition may be formed using molecular beam epitaxy (MBE), sputtering, or any other method which produces an approximately conformal coverage of the surface of the HFET. Many other surfaces may also be coated with AlN, including silicon devices, nitride devices, GaN based LEDs and lasers as well as other semiconductor systems.

The deposition is performed at approximately 150°C and uses alternating beams of aluminum and remote plasma RF nitrogen to produce an approximately 500Å thick AlN layer. The temperature and thickness may be varied as desired. At temperatures

about or higher than 300°C, melting may occur, damaging the integrity of the HFET. Lower temperatures may also be used, and in fact may provide desired crystalline characteristics.

Using MBE, alternating periods of deposition of Al and N are approximately two seconds in length, with two second intervals between the depositions. The times may be varied significantly, but approximate migration enhanced epitaxy, which may also be used. Such deposition provides highly conformal coverage of the passivation layer on the gate between source and drain ohmic contacts.

HFETs with AlN passivation layers are useful in a wide range of products, including microwave generated plasma lights, microwave transmitters, receivers, cellular base stations, microwave ovens, home to satellite transceivers, and collision avoidance radar for automobiles to name a few.